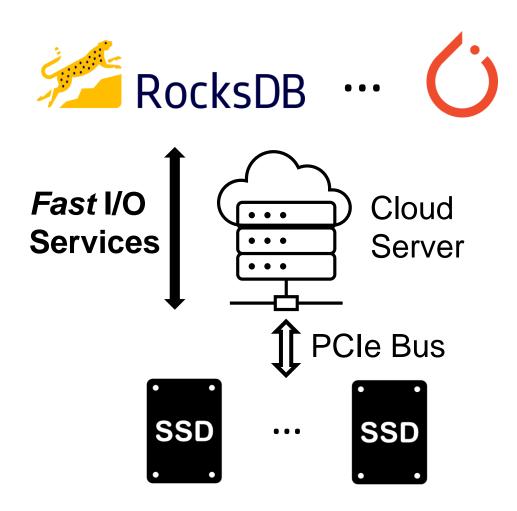
Daredevil: Rescue Your Flash Storage from Inflexible Kernel Storage Stack

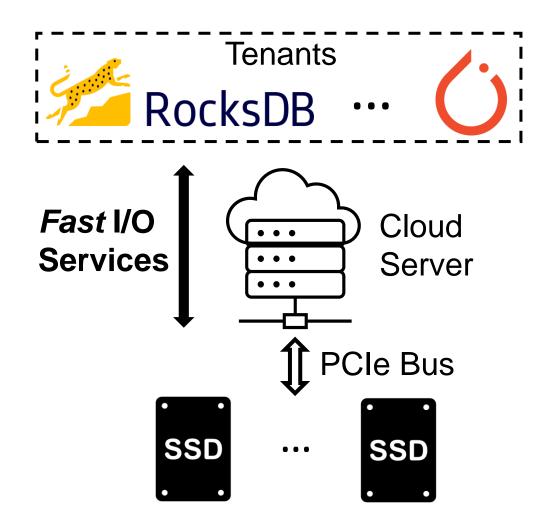
Junzhe Li, Ran Shu, Jiayi Lin, Qingyu Zhang, Ziyue Yang, Jie Zhang, Yongqiang Xiong, Chenxiong Qian



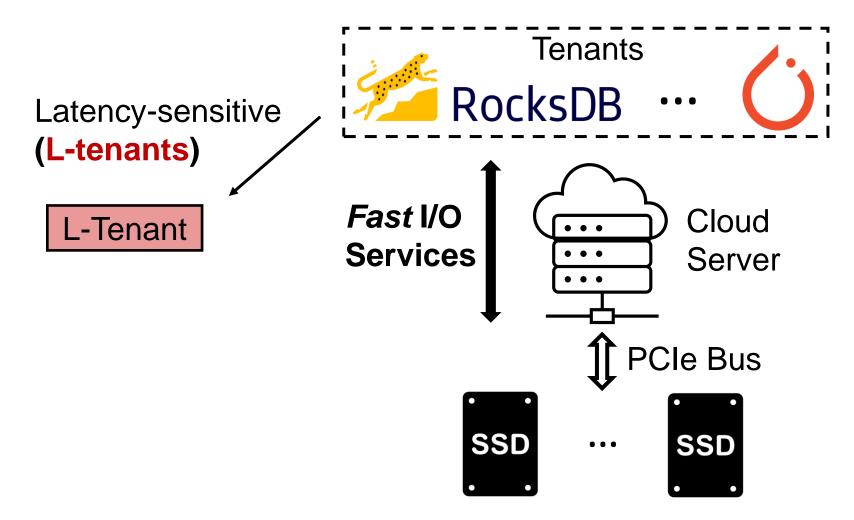




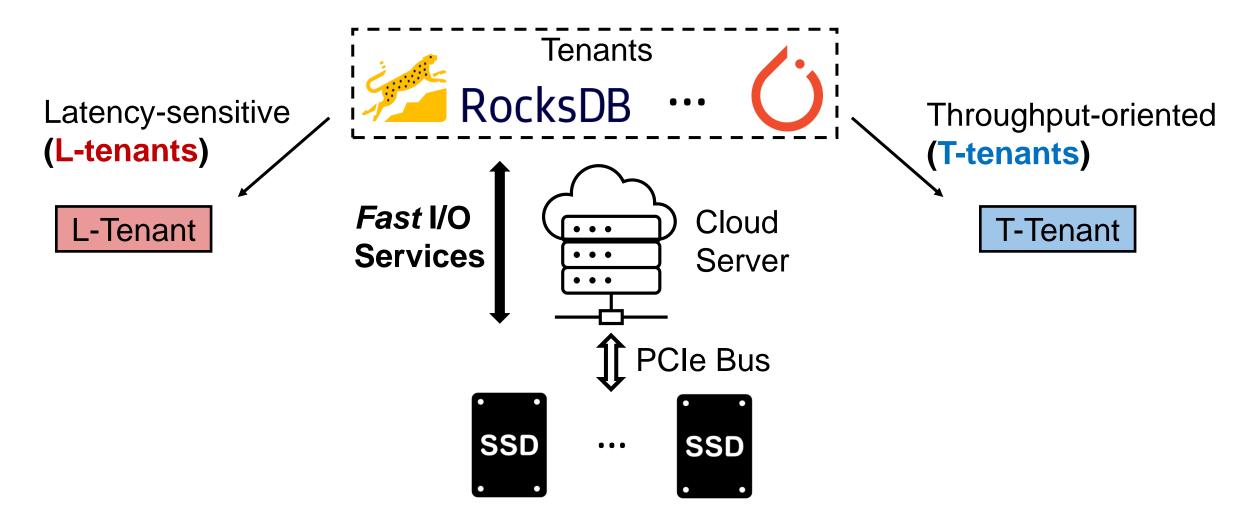




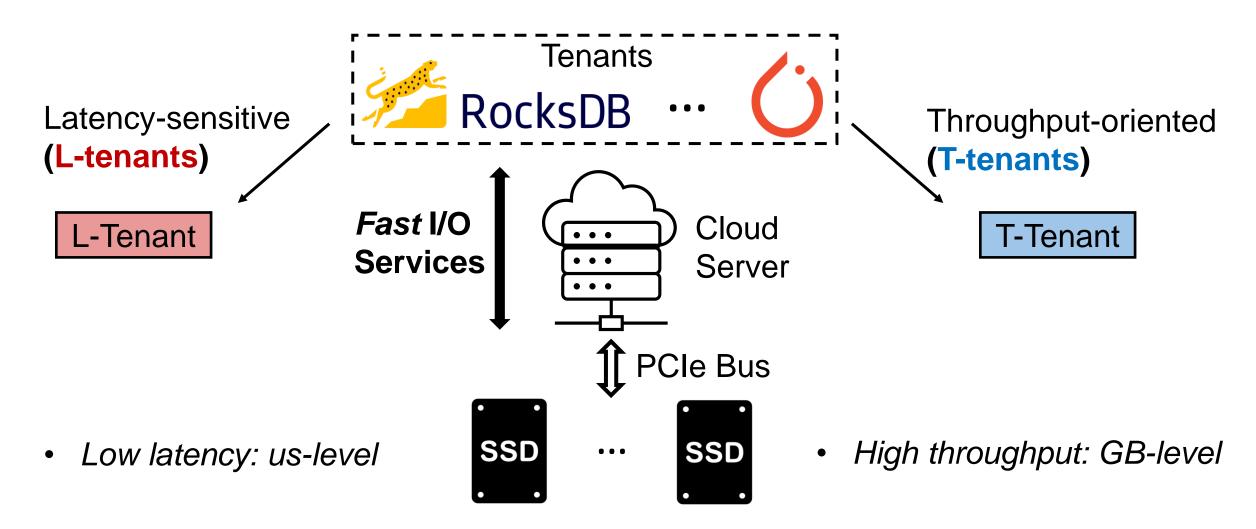
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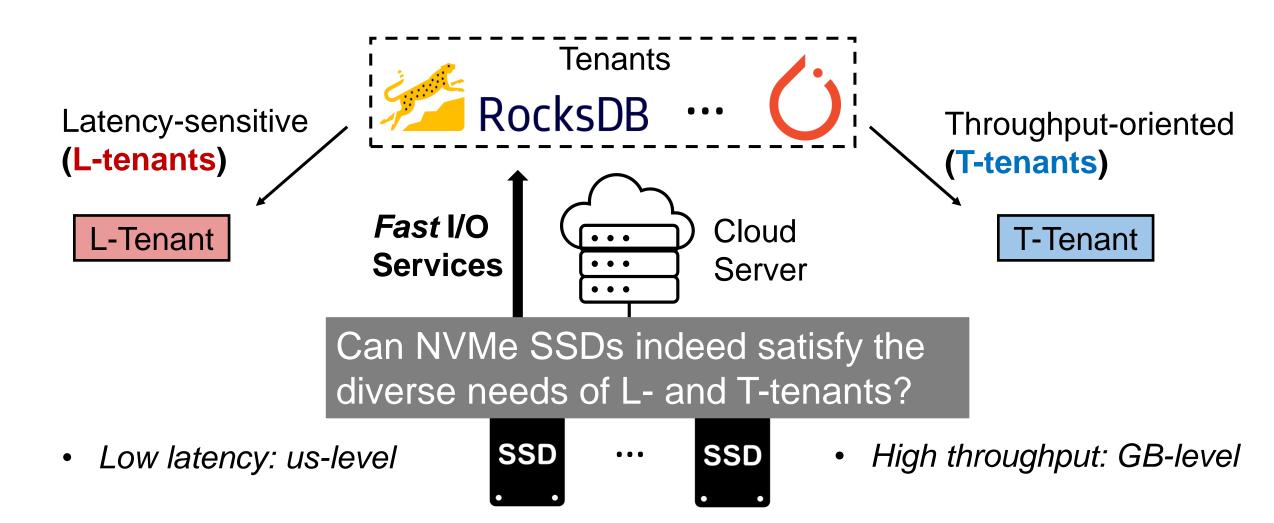
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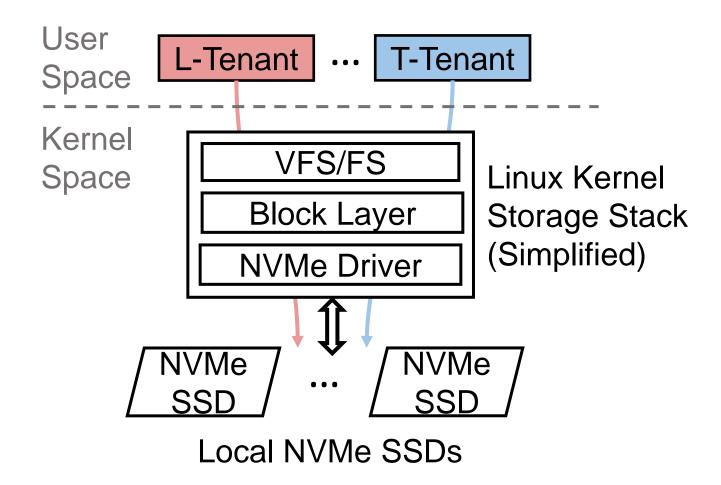
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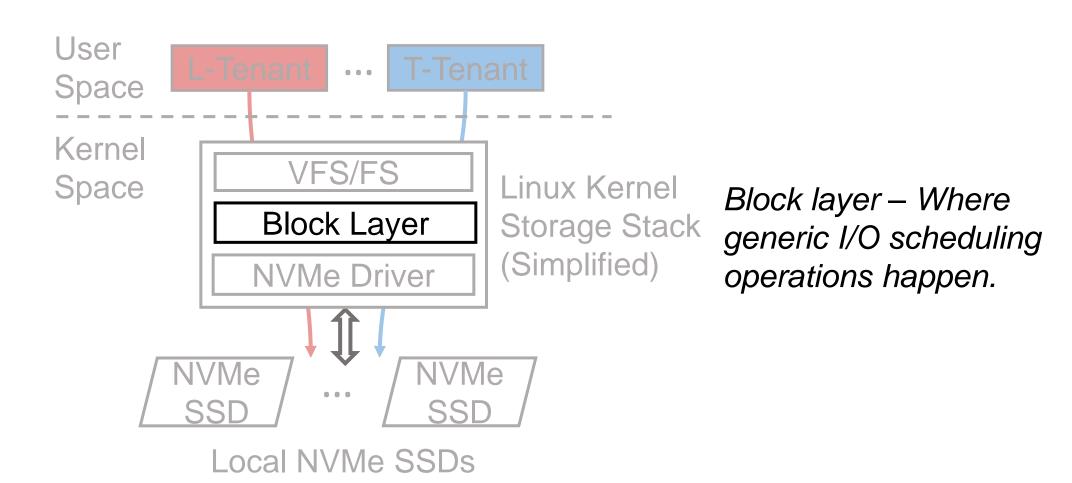
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I/O Services: In the Eyes of the Kernel



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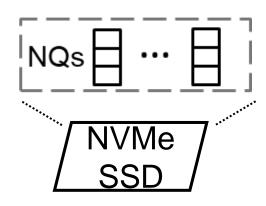


NVMe SSDs support multiple NVMe I/O queues (NQs)

- Used for kernel-SSD I/O interactions
- Parallel access supported

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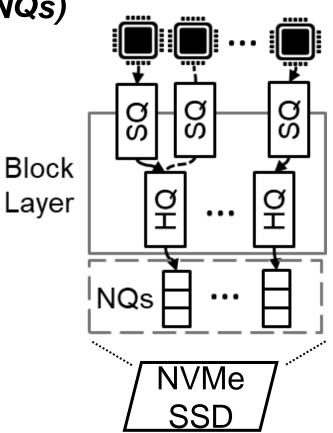
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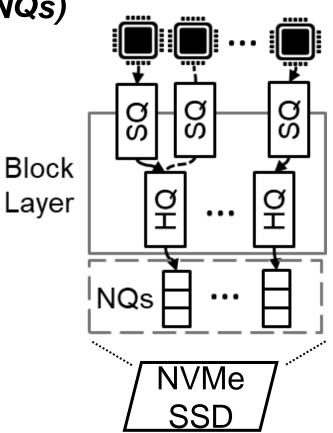


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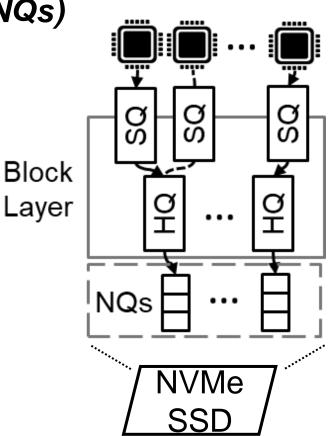


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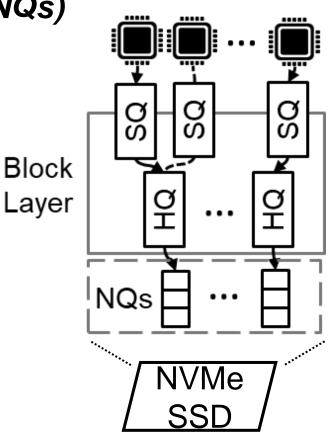


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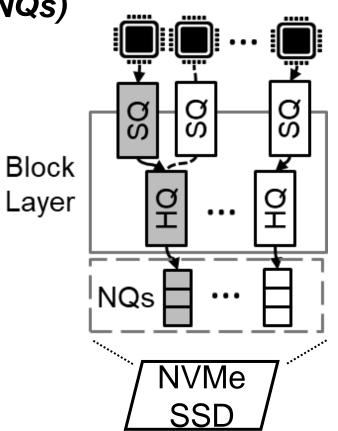


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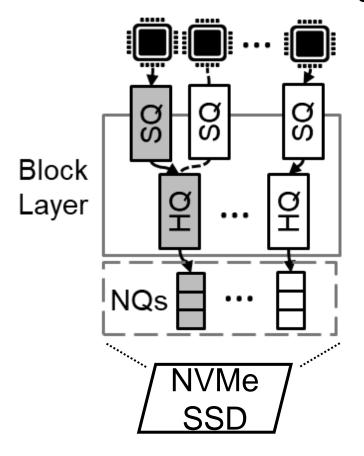
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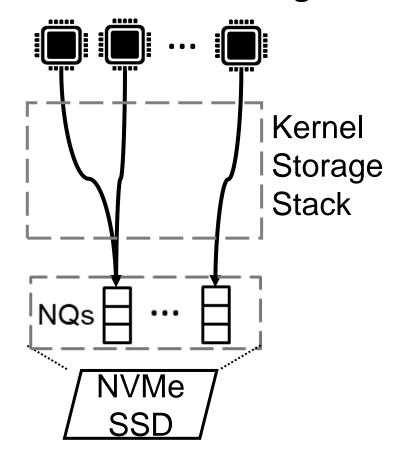
I/O flow: CPU core \rightarrow SQ \rightarrow HQ \rightarrow NQ

Static SQ-NQ bindings

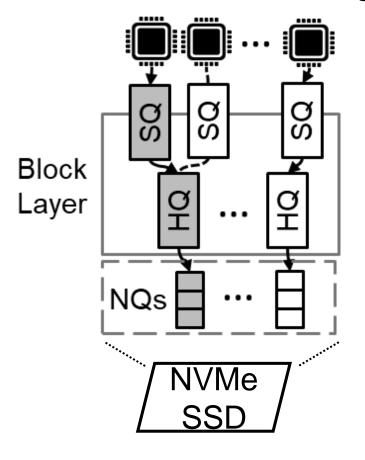


Essence of blk-mq:

Static CPU-NQ bindings



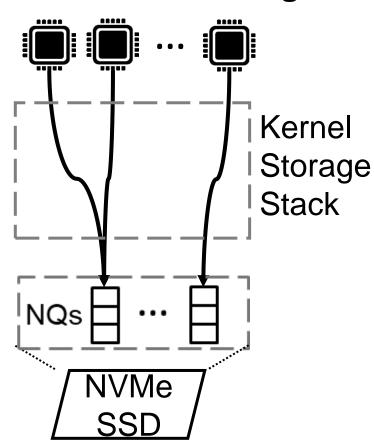
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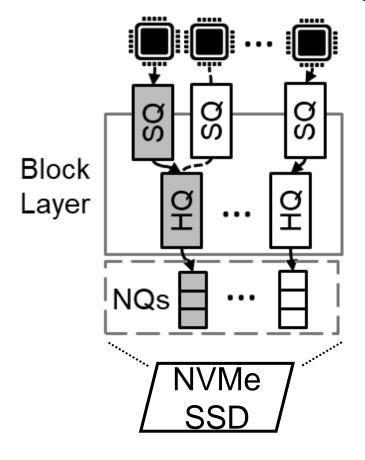
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- Maintenance
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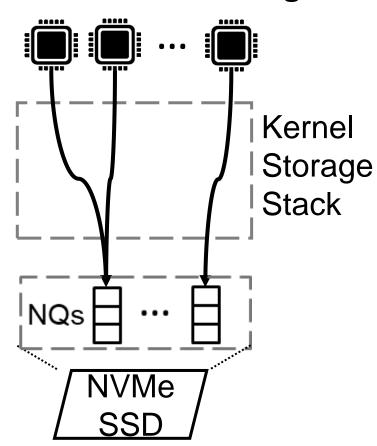
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Essence of blk-mq:

- Maintenance
- Parallelism/Concurrency
- But...! Troublesome in cloud servers

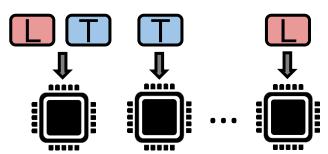
Static CPU-NQ bindings



T: Throughput-oriented tenants (T-tenant)

L : Latency-sensitive tenants (L-tenant)

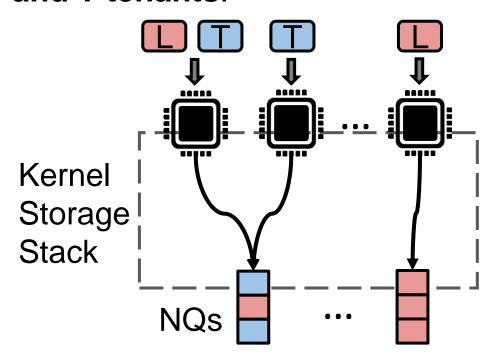
Common CPU sharing among L-and T-tenants.



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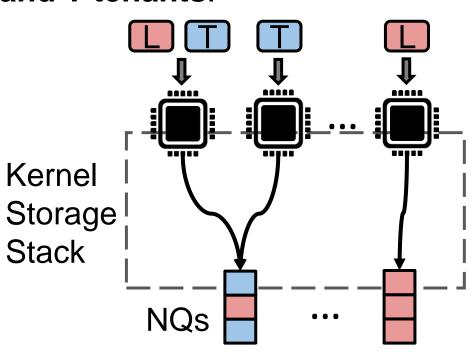
Small I/O Size Large

L-requests T-requests Storage

Quick Processing Time Slow

Kernel Storage Storage Stack

Common CPU sharing among L-and T-tenants.



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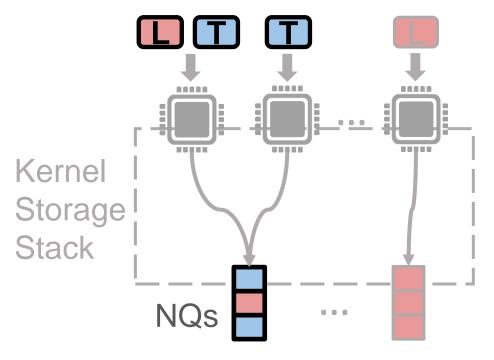
Kernel

T-requests

Storage

Stack

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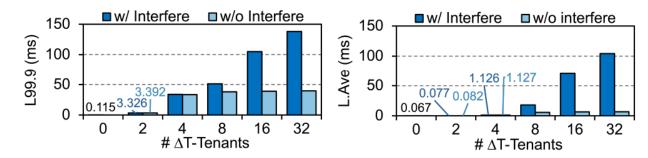
Head-of-line (HOL) blocking from T-requests!

Experiment:

- w/ Interfere: L- and T-tenants served within the same NQs.
- w/o Interfere: L- and T-tenants served by separate NQs.

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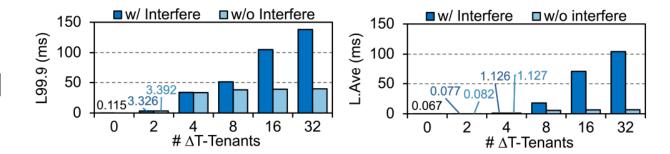
- (a) L-tenant 99.9^{th} tail latency.
- **(b)** L-tenant average latency.

Figure 2. I/O latency of L-tenants with T-tenants interfering within the same NQs (*w*/ *Interfere*) and using separate NQs (*w*/o *Interfere*).

3x/15x increase in tail/average latency with HOL T-requests.

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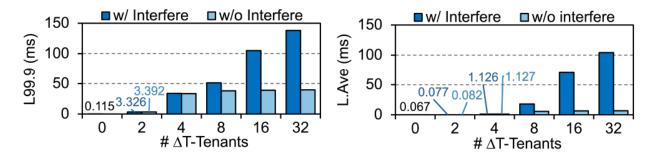
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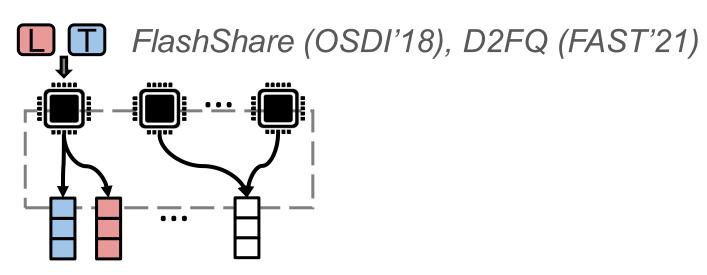
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How can we solve this issue within the kernel storage stack?

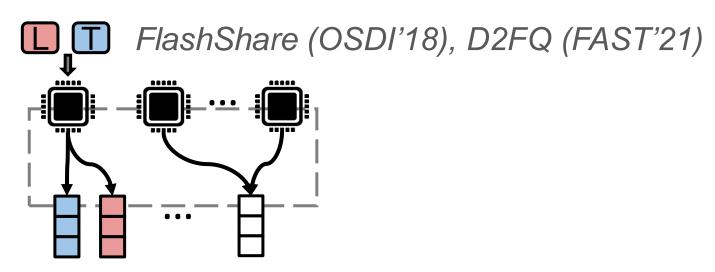
Clear solution: **NQ-level separation** of L- and T-requests.

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NQ overprovision:

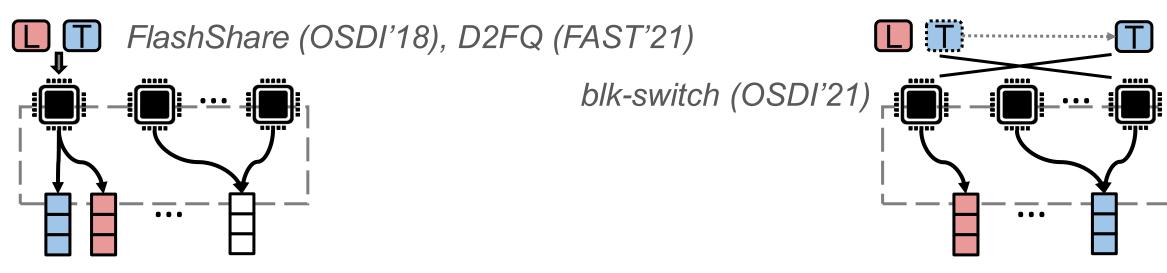
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NQ overprovision:

- Simple & Direct
- Underutilization & HW constraints

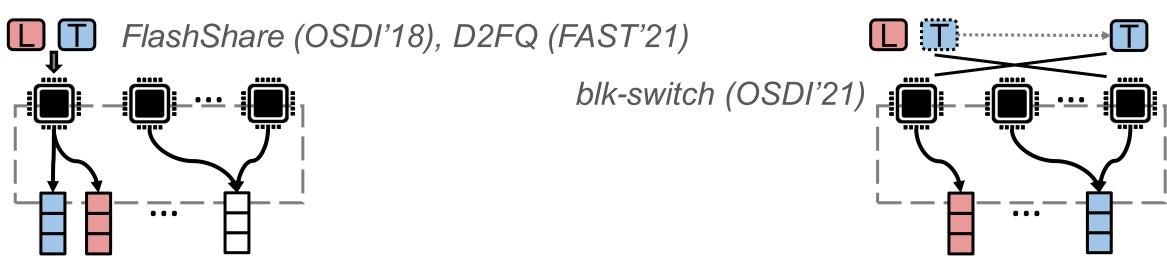
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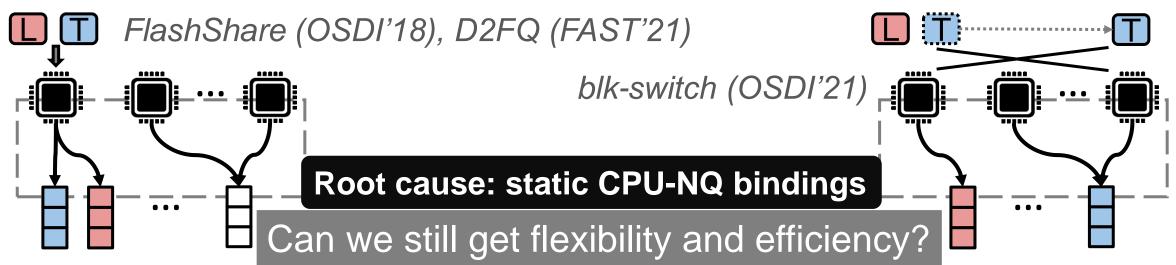


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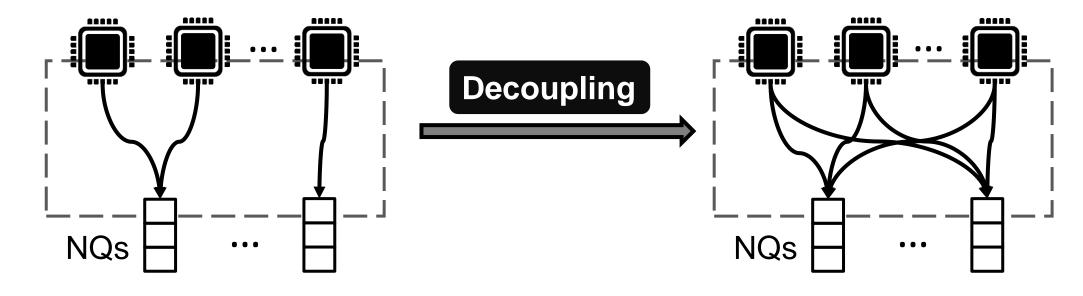
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Daredevil: Here Comes the Rescue

Core idea: **Decoupling** of CPU-NQ bindings.

Daredevil: Here Comes the Rescue

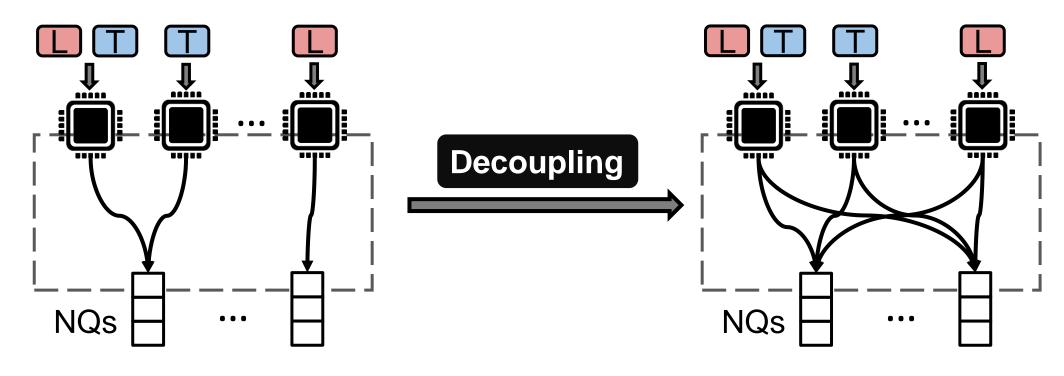
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blk-mq based storage stack

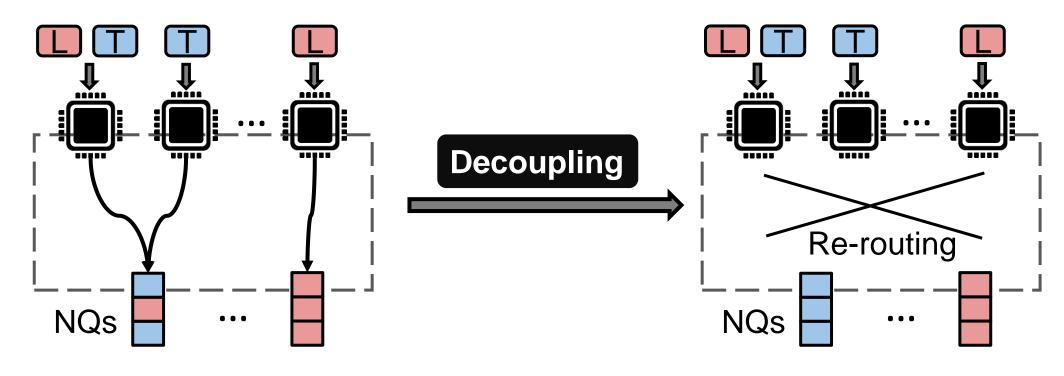
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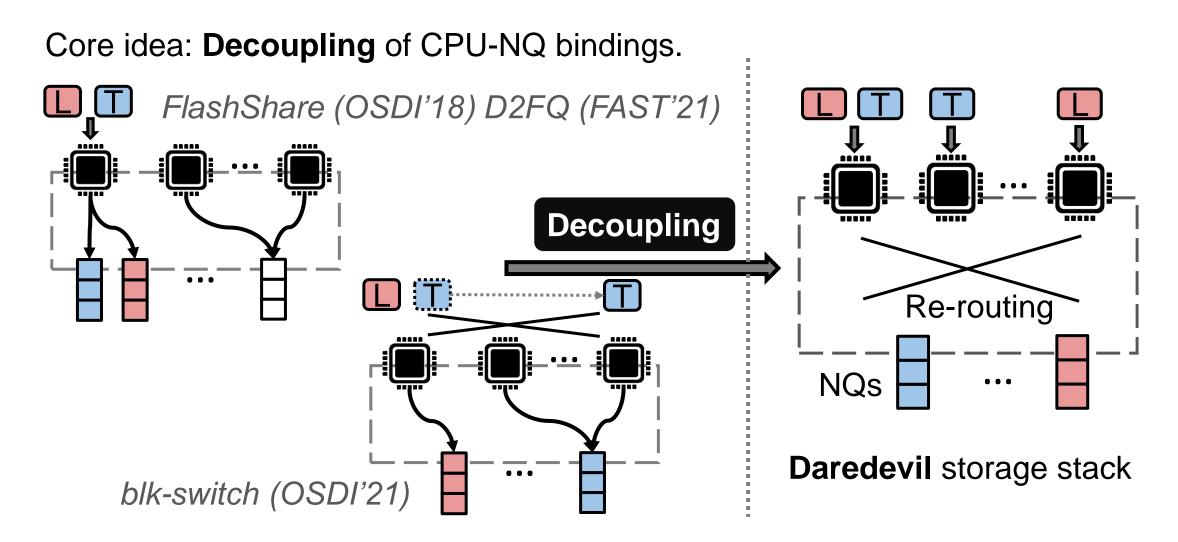


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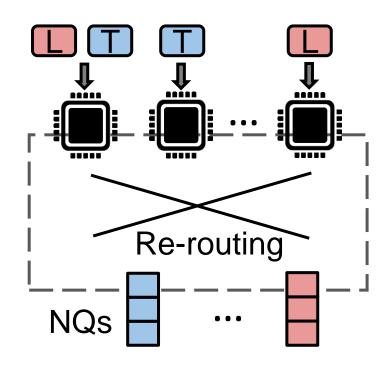


Core idea: **Decoupling** of CPU-NQ bindings.

Full-connectivity between CPU cores and NQs.

 Independent & flexible policy for multi-tenancy control.

Full utilization of NQs.



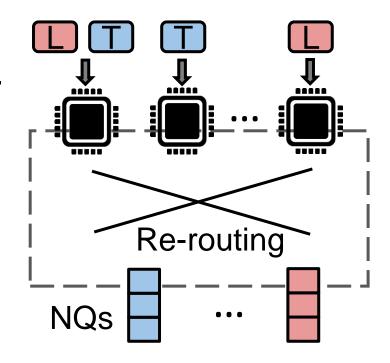
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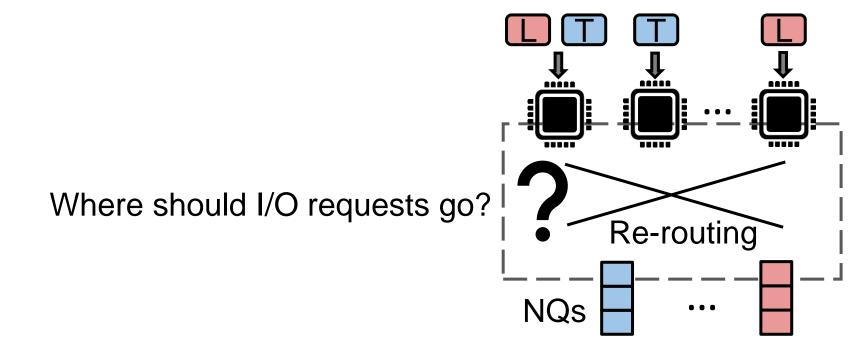
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But...At what cost?

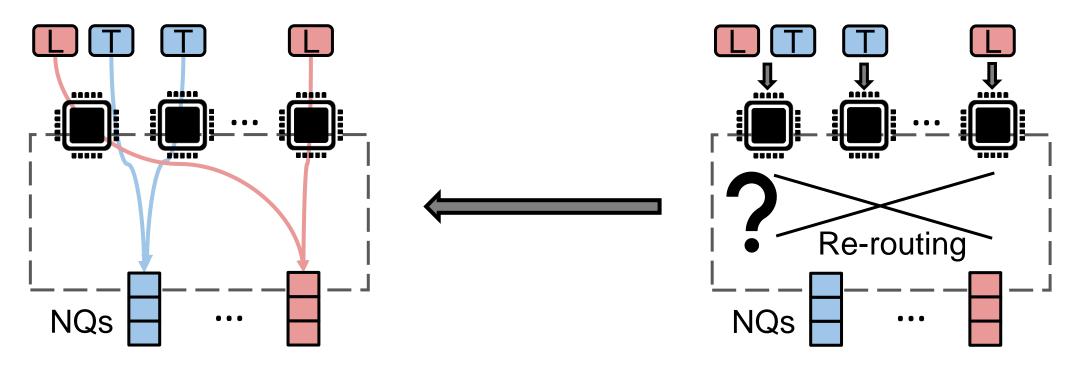
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Challenge #1: Light-weight routing decisions for I/O requests.

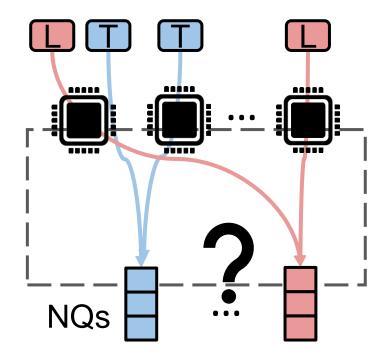


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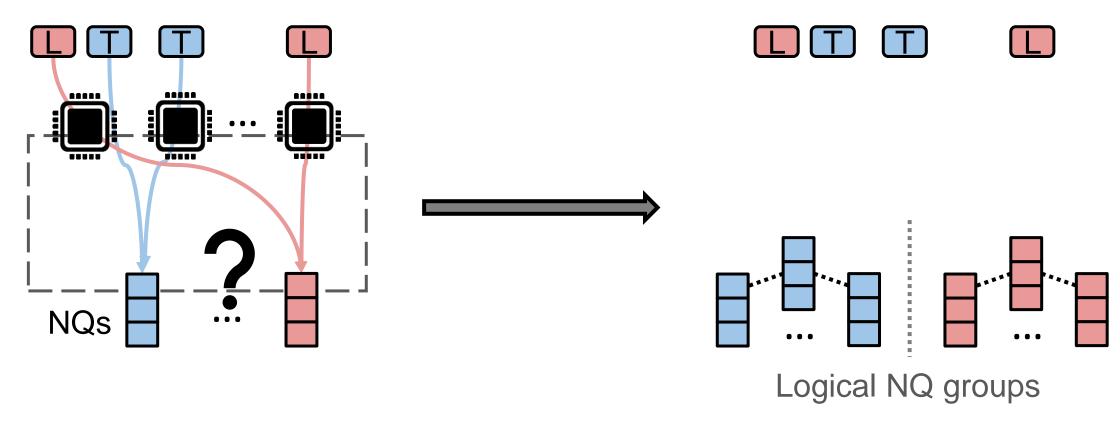
Solution #1: Tenant-based request routing.

Challenge #2: Performance assurance for NQ-level separation.



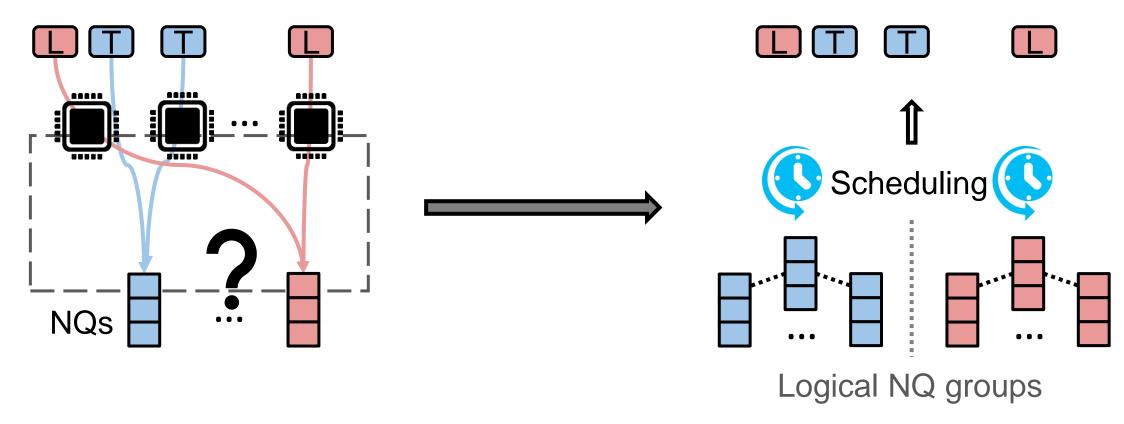
How to ensure separation with guaranteed performance?

Challenge #2: Performance assurance for NQ-level separation.



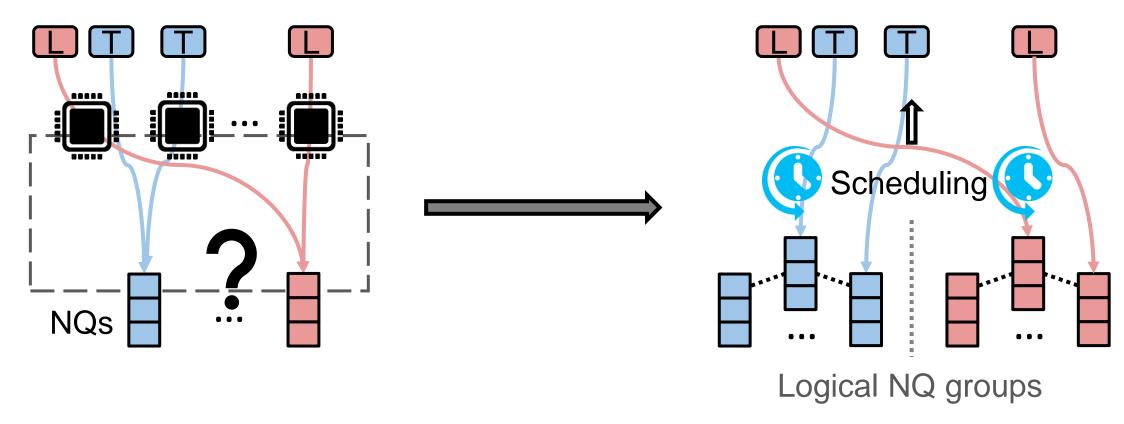
Solution #2: Heap-based performance-aware NQ scheduling.

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Design & implementation details:

Tenant & outlier cases identification

Scheduling criteria

Please refer to our paper for more details.

Light-weight concurrent scheduling

I/O service acceleration

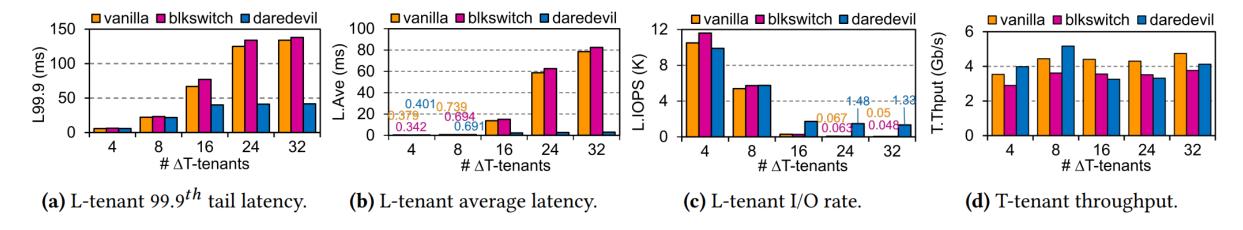


Figure 6. Performance results with increasing T-pressure in SV-M. DAREDEVIL maintains in-time responses for L-tenants even under extreme T-pressure, while the vanilla kernel and blk-switch significantly inflate the L-tenants' I/O latency.

Benchmark: FIO-based simulation for L- and T-tenants.

3x & 27x reduction in tail & ave latency.

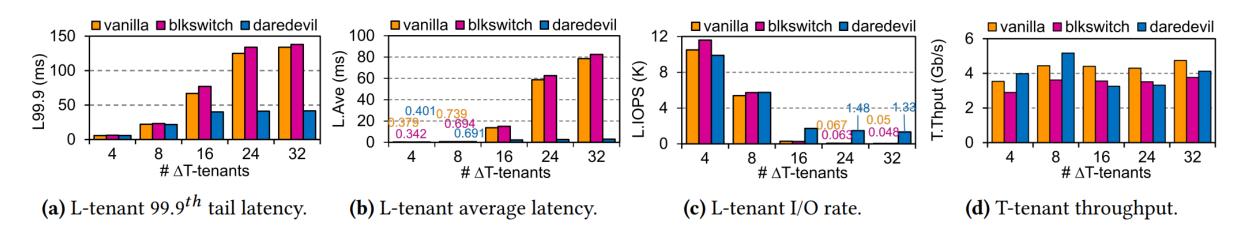
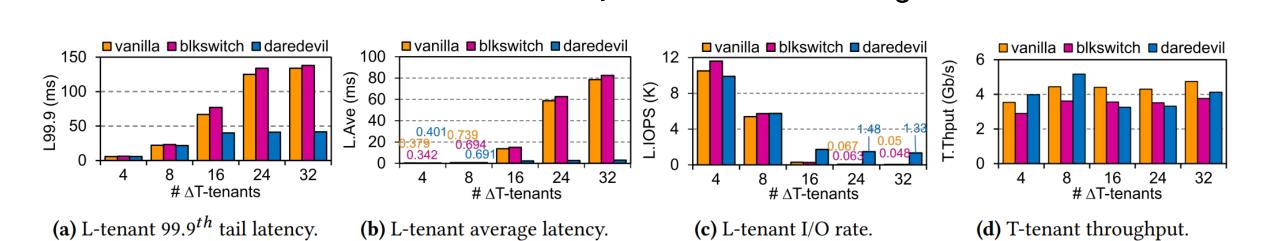


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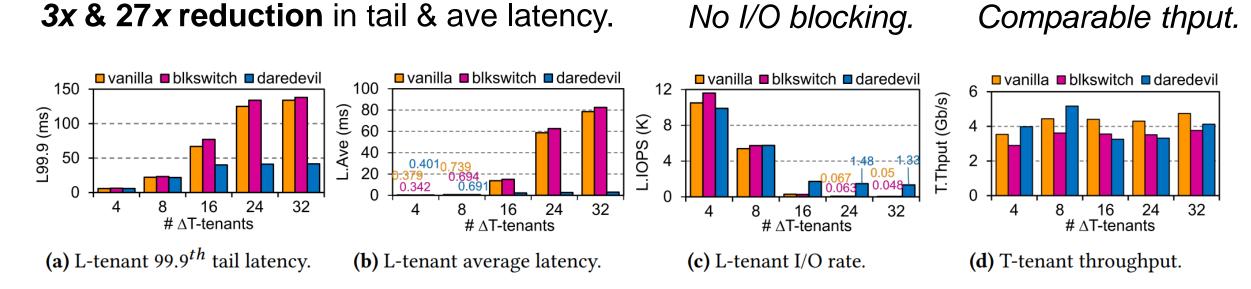


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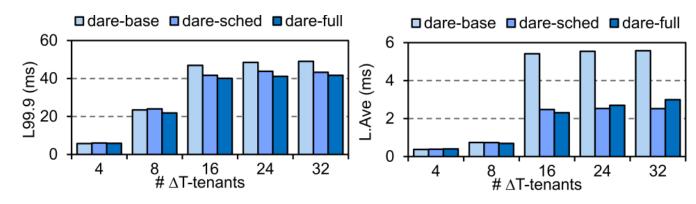
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Ablation of Daredevil: What contributions do its optimizations make?

- dare-base: only decoupling and round-robin request routing
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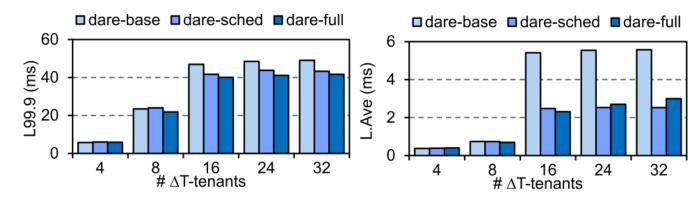


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 Decoupled block layer already achieves low latency.

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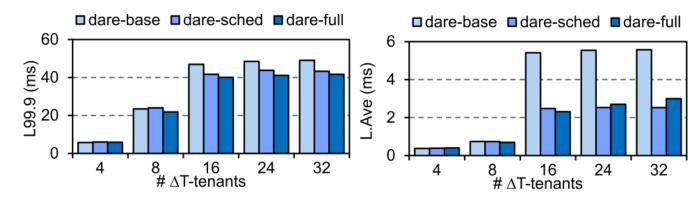


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- Decoupled block layer already achieves low latency.
- NQ scheduling significantly contributes.
- I/O service acceleration reduces tail latency.

Discussion

Compatibility with virtual machines (VMs)?

Not yet: processes inside VMs are invisible to the host.

Beyond NVMe SSDs to new devices?

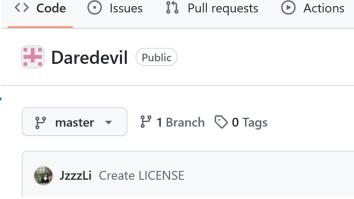
Possible: the multi-queue feature is maintained for CXL/ZNS SSDs.

Future road after Daredevil:

- Finer-grained performance isolation/consideration with cgroups.
- More comprehensive maintenance with CPU core scheduling.

Conclusion

- Daredevil is a wild research prototype to challenge the static Linux kernel storage stack.
- It achieves flexibility and efficiency with higher performance multi-tenant I/O services.
- Open sourced at: https://github.com/HKU-System-Security-Lab/Daredevil



Please contact Junzhe Li (jzzzli@connect.hku.hk) for any questions!

Thank you!